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# Study of Improved Topologies of Nanowire MOSFET: Solution to Doping Control Issues

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***Abstract*—As we know that technology is improving day by day, due to this the number of transistors on chip should be doubled every year as per "Moore's Law". Hence, the size of transistor should be reduced to follow this scaling trend but using conventional planar MOSFET we cannot reduce the size of transistor to a limit. This is happened because of short channel effects (SCEs), which degrades MOSFET performance at lower dimensions. But there are many alternate structures like nanotube, nanowire, graphene etc. which will help in reducing the size of transistor by offering lower SCEs. In this paper, we will discuss about various types of nanowire MOSFETs and their analog performances like $I_{ON}$, $I_{OFF}$, $I_{ON}/I_{OFF}$ current ratio. Beside this, an in depth review of doping control issues and the possible solutions in the nanowire MOSFETs are also presented.**

***Index Terms*— nanowire, short channel effects.**

## I. INTRODUCTION

There are various short channel effects like leakage current, heat dissipation, band to band tunneling, gate induced drain leakage effects develop in MOSFET due to scaling down MOSFET in nanometer regime [1]. These effects are reduced by nano-scaled devices like nanowire. Nanowire (NW) MOSFET has various advantages over bulk MOSFET such as less power dissipation, higher speed and higher packaging density [2]. We know that with increase in number of gate in MOSFET, electrostatic control over channel increases, hence nanowire has highest electrostatic control over channel due to having multi gate structure [2]. There are two approaches for fabricating nanowire (1) top-bottom approach (2) bottom-top approach. Top–bottom approach is done by advanced lithography with dry/wet etching whereas bottom-top approach is done by chemical vapour deposition (CVD). Bottom-up approach for fabricating nanowire has higher advantages over top-bottom approach like cost effective and higher quality [2]. Nanowire has been researched on both junction based and junctionless devices [3,8,9]. Junction based nanowire MOSFET has abrupt junction between drain/source and silicon body [5]. Due to ultrasharp junction creation between source/drain and silicon body, magnitude of doping concentration in junction based device changes with distance of some nananometer [14]. Hence there is a need of ultrafast dopant activation process and highly precise doping techniques. Junctionless nanowire MOSFET is free from junctions and has constant doping concentration in source, channel and drain areas [10-13]. Junction based nanowire MOSFET comes under category of inversion-mode MOSFET whereas junctionless nanowire MOSFET uses the mechanism for carrier transportation that why junctionless nanowire MOSFET termed as accumulation- mode MOSFET [5].

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Junctionless device has lots of advantages over junction based device like excellent short channel immunity and less OFF current [10,15,16,17,18]. but because of using highly doping concentration in source, drain and channel, junctionless device suffers from random dopant fluctuation (RDF) effects like threshold voltage variations [4], subthreshold swing and variation in analog performance like decrease mobility of carrier, decrease on-state ($I_{ON}$) current [7], decrease transconductance [7,19,20]. To solve these problems, charge plasma based dopingless nanowire MOSFET is proposed. Charged plasma technique uses appropriate work function of source, drain and gate metal electrode as well as lightly doping on silicon body for the formation of source/drain region whereas in junctionless device, accumulation of electrons at edge of source and drain region are done by using heavy doping in silicon body as well as appropriate work function.

Charge plasma technique has already proposed for various other devices like bipolar junction transistor [23] and p-n junction diode [21]. There are great advantages of using charge plasma technique like reduction in fabrication cost and thermal budget [25]. Shan et al. [24] showed the fabrication processing steps for charge plasma based MOSFET [4].

In this paper, various improved topologies of nanowire MOSFET is discussed and compared. Different improved topologies will help in to solve doping control issues as well as enhance analog performances like increased $I_{ON}$ current, reduced $I_{OFF}$ current and subthreshold slope etc. In the second section of this paper, conventional junction based nanowire is discussed. In the third section, improved structure of nanowire is discussed which is used to reduce doping problems. In the forth section conclusion of this paper is discussed.

## II. Conventional Junction based Nanowire

Conventional Junction based nanowire is inversion-mode MOSFET [5]. From study of Ref. [ 3], it is found that conventional junction based nanowire uses channel doping of $1 \times 10^{14}$ $cm^{-3}$ whereas source/drain doping of $1 \times 10^{20}$ $cm^{-3}$ [3]. Remaining parameter i.e. body thickness = 32 nm and channel length = 45 nm [3]. 3D structure for conventional device is shown in Fig.1. Analog performance for the device like that $I_{ON}$ current and $I_{OFF}$ current for conventional junction based nanowire is $3.09 \times 10^{-3}$ A and $1.04 \times 10^{-7}$ A at gate work function of 4.4 eV [3] . Moreover, due to have abrupt junctions and variation in doping concentration between drain, source and channel, conventional device has high series resistance [5] which reduced overall performance of device. Therefore, there are many devices have been designed to solve the problem of doping control and abrupt junctions. These types of improved devices will be discussed in next section.

## III. Improved Structures to Control Doping Problems and Enhance Analog Performance

### *A. Junctionless and Dopingless Nanowire MOSFET*

Fig. 2 shows the 2D cross-section view of junctionless and dopingless nanowire MOSFET [4]. From study of Ref. [4], it is found that channel/drain/source doping for both device junctionless nanowire and dopingless nanowire is $1 \times 10^{19}$ $cm^{-3}$, and $1 \times 10^{15}$ $cm^{-3}$ respectively whereas remaining parameter for both device remains same such as body thickness is 10nm ,length of channel is 20nm [4] .Both junctionless and dopingless nanowire mosfets are the accumulation-mode MOSFET. In both devices source and drain regions induced by accumulation of electron. In dopingless nanowire MOSFET, accumulation of electron is done by charge plasma concept. Due to having uniform doping concentration between source/drain and channel, these devices have no abrupt junction formation hence reduce series resistance as well as analog performances are such that $I_{ON}$ current for both devices junctionless nanowire MOSFET and dopingless nanowire MOSFET is $\sim 10^{-5}$ A at gate work function of 5.1 eV and 4.8 eV respectively [4].

$I_{OFF}$ current for both devices junctionless nanowire MOSFET and dopingless nanowire MOSFET is $\sim 10^{-14}$ A and $\sim 10^{-15}$ A at gate work function of 5.1 eV and 4.8 eV respectively [4]. $I_{ON}/I_{OFF}$ current ratio for junctionless and dopingless nanowire MOSFET is $6.29 \times 10^{8}$ A and $3.23 \times 10^{9}$ A respectively at body thickness of 10 nm [4].

*B. Gate Stacked Junctionless and Dopingless Nanowire MOSFET*

Fig. 3 shows 2D cross-sectional view of gate stacked junctionless nanowire MOSFET and gate stacked dopingless nanowire MOSFET. From Ref. [5], device structure parameters used for both devices are such as, length of gate is 20 nm, body thickness is 10 nm, spacer length is 10 nm, doping concentration used for gate

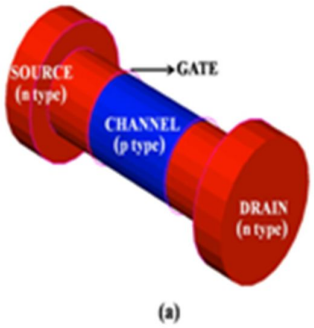


Figure 1(a) 3D structural view of conventional Junction based nanowire MOSFET [3].

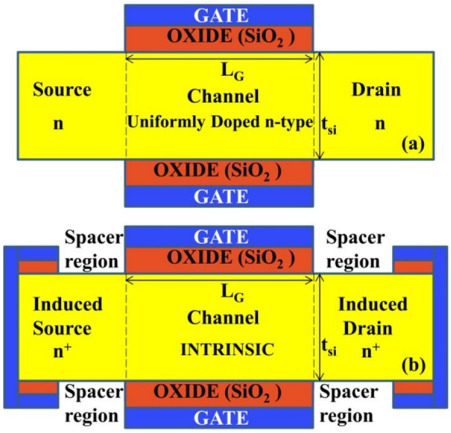


Figure 2. 2D cross-sectional view of (a) Junctionless nanowire MOSFET (b) Dopingless nanowire MOSFET [4].

stacked junctionless and dopingless nanowire is $1x10^{19}$ $cm^{-3}$, and $1x10^{15}$ $cm^{-3}$ respectively. In the paper Ref. [4], only oxide material is used in gate which cannot control static power dissipation and leakage current in device but from study of Ref. [5], it is observed that a high-k material is added under gate metal electrode and above oxide layer in sandwich like structure helps to reduce leakage current and power dissipation by reducing formation of gate capacitance [5].HfO2 material is also under drain and source metal electrode to reduce silicide formation [5]. Analog performances for both devices are such that $I_{ON}$ current for both devices gate stacked junctionless nanowire MOSFET and gate stacked dopingless nanowire MOSFET is ~ $2x10^{-5}$ A and ~ $6x10^{-5}$ A at gate work function of 4.7 eV and 4.53 eV respectively [5]. $I_{OFF}$ current for both devices junctionless nanowire MOSFET and dopingless nanowire MOSFET is ~$3x10^{-10}$ A and ~$1x10^{-10}$ A at gate work function of 4.7 eV and 4.53 eV respectively [5].$I_{ON}/I_{OFF}$ current ratio for junctionless and dopingless nanowire MOSFET is ~$0.6x10^{5}$ A and ~$6x10^{5}$ A respectively at body thickness of 5 nm. In both devices, air is used in spacer [5].

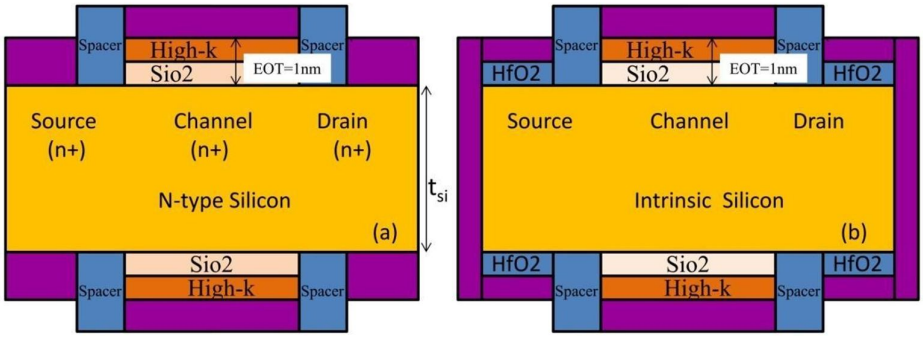


Figure 3. 2D cross-section view of (a) gate stacked junctionless nanowire MOSFET (b) gate stacked dopingless nanowire MOSFET [5]

*C. Dual Material Gate and Gate Stacked Junctionless and Dopingless Nanowire MOSFET*

Fig. 4 shows 2D Cross- sectional view of both devices dual material gate and gate stacked junctionless nano-wire MOSFET and dual material gate and gate stacked dopingless nanowire MOSFET. From Ref. [6], structure parameter used in both devices are length of gate (LM1 +LM2 =20nm), spacer length is 10 nm, body thickness is 10 nm, doping concentration used for gate stacked junctionless and dopingless nanowire is

$1x10^{19}$ $cm^{-3}$, and $1x10^{15}$ $cm^{-3}$, respectively. Dual material is used on gate metal electrode to enhance the analog performance for both devices. In both devices, work function of both material used in gate metal electrode are differ by 0.5 eV [6].And using high-k material on top of oxide layer decreases leakage current and power dissipation by reducing formation of gate capacitances [5]. In both devices HfO2 is used under source and drain metal electrode to avoid silicide formation [5]. Analog performances are such that $I_{ON}$ current for both devices such as dual material gate stacked junctionless nanowire MOSFET and dual material gate stacked dopingless nanowire MOSFET is ~2 x $10^{-4}$A and ~4 x $10^{-4}$ A at gate work function of M1=4.91 eV, M2=4.41 and M1= 4.77 eV, M2=4.27 eV respectively [6]. $I_{OFF}$ current for both devices such as dual material gate stacked junctionless nanowire MOSFET and dual material gate stacked dopingless nanowire MOSFET is almost equal

i.e. ~5 x $10^{-13}$ A at gate work function of M1=4.91 eV, M2=4.41 and M1= 4.77 eV, M2=4.27 eV respectively [6].

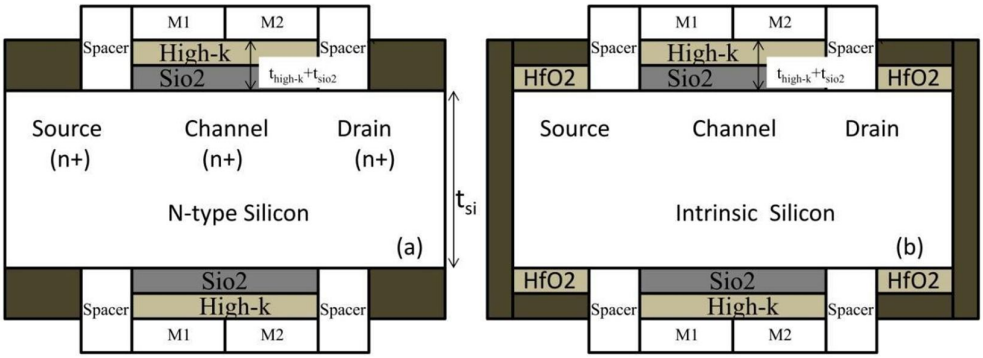


Figure 4. 2D cross-sectional view of (a) dual material gate and gate stacked junctionless nanowire MOSFET (b) dual material gate and gate stacked dopingless nanowire MOSFET [6]

TABLE I. COMPARISON OF VARIOUS PARAMETERS FOR DIFFERENT WORKS

| S. NO | Device | Structure Parameters | | | | | | Analog Characteristics | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Channel Length (nm) | Body thickness (nm) | $t_{ox}$ (nm) | Gate Work Function (eV) | Channel Doping ($cm^{-3}$) | urce/drain Doping ($cm^{-3}$) | $I_{ON}$ (A) | $I_{OFF}$ (A) | $I_{ON}$ /$I_{OFF}$ |
| 1. | Conventional Junction based Nanowire | 45 | 32 | 1 | 4.4 | $1x10^{14}$ | $1x10^{20}$ | $3.09 x10^{-3}$ | $1.04 x10^{-7}$ | $2.98 x10^{4}$ |
| 2. (A) | Junction less Nanowire | 20 | 10 | 2 | 5.1 | $1x10^{19}$ | $1x10^{19}$ | $\sim10^{-5}$ | $\sim10^{-14}$ | $6.29 x10^{8}$ |
| 2. (B) | Doping Less Nanowire | 20 | 10 | 2 | 4.8 | $1x10^{15}$ | $1x10^{19}$ | $\sim10^{-5}$ | $\sim10^{-15}$ | $3.23 x10^{9}$ |
| 3. (A) | Gate Stacked Junction Less Nanowire | 20 | 10 | 1 | 4.7 | $1x10^{19}$ | $1x10^{19}$ | ~ 2 x $10^{-5}$ | ~ 3 $x10^{-10}$ | ~ $0.6 x10^{5}$ |
| 3. (B) | Gate Stacked Doping Less Nanowire | 20 | 10 | 1 | 4.53 | $1x10^{15}$ | $1x10^{15}$ | ~ 6 x $10^{-5}$ | ~ 1 x $10^{-10}$ | ~ $6 x10^{5}$ |
| 4. (A) | Dual Material Gate Stacked Junction Less Nanowire | 20 | 10 | 1.1 | 4.91, 4.41 | 1 x $10^{19}$ | 1 x $10^{19}$ | ~2 x $10^{-4}$ | ~5 x $10^{-13}$ | ~0.4 x $10^{9}$ |
| 4. (B) | Dual Material Gate Stacked Doping Less Nanowire | 20 | 10 | 1.1 | 4.77, 4.27 | 1 x $10^{15}$ | 1 x $10^{15}$ | ~4 x $10^{-4}$ | ~5 x $10^{-13}$ | ~0.8 x $10^{9}$ |

## IV. Conclusions

There are many studies going on day by day on nanowire MOSFET device to reduce its size, leakage current, power dissipation and SCEs thereby improve its speed and performance parameters such as $I_{ON}$, $I_{OFF}$, $I_{ON}/I_{OFF}$ ratio etc. In this paper, we have summarized the various studies held on nanowire MOSFET to control its doping problem and enhance analog performance. Various researchers are now working on nanowire devices to further enhance overall performance of devices and able to sustain "Moore's Law" as nanowire structures have the potential to build future nanodevices.


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